UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/806,379	03/23/2004	Jang-Kun Song	8071-128T (OPP 030152US)	1832

7590 10/04/2006

F. Chau & Associates, LLC
130 Woodbury Road
Woodbury, NY 11797

EXAMINER	
NGUYEN, THANH NHAN P	
ART UNIT	**PAPER NUMBER**
2871	

DATE MAILED: 10/04/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/806,379	SONG, JANG-KUN	
	Examiner	Art Unit	
	(Nancy) Thanh-Nhan P. Nguyen	2871	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 September 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-40* is/are pending in the application.

4a) Of the above claim(s) *26-36* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-25 and 37-40* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *23 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Applicant's request for reconsideration of the finality of the rejection of the last Office action is persuasive (English translation provided), and therefore, the finality of that action is withdrawn.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-9, 12, 23 and 37-40 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ochiai et al (US 6,897,909) in view of Nishimura et al (US 2006/0050220).

Regarding claim 1, Ochiai et al discloses a thin film transistor array panel comprising: a substrate (GLS1); a plurality of first signal lines (GL) formed on the substrate, extending in a first direction, and separated from each other by a predetermined interval; a plurality of second lines (DL) formed on the substrate, intersecting the first signal lines, a plurality of pixel electrodes (SPT) located substantially in areas defined by the first and the second signal lines; and a plurality of thin film transistors connected to the first and the second signal lines and the pixel electrodes, [figs. 1 & 3].

Ochiai et al lacks disclosure of the second lines including a plurality of curved portions and intermediate portions extending in a second direction and alternately

arranged by the predetermined interval, wherein the intermediate portions intersect the first signal lines and extend from the curved portions at an angle with respect to the curved portion.

Nishimura et al discloses second lines (DL) including a plurality of curved portions and intermediate portions extending in a second direction and alternately arranged by the predetermined interval, wherein the intermediate portions intersect the first signal lines (GL) and extend from the curved portions at an angle with respect to the curved portion, [fig. 8], for the benefit of being possible to obtain multi-domain effect as well as the effect of reducing a parasitic capacity, [par. 0229]. Therefore, at the time the invention was made, it would have been obvious to a person of ordinary skill in the art to have second lines including a plurality of curved portions and intermediate portions extending in a second direction and alternately arranged by the predetermined interval, wherein the intermediate portions intersect the first signal lines and extend from the curved portions at an angle with respect to the curved portion for the benefit of being possible to obtain multi-domain effect as well as the effect of reducing a parasitic capacity.

Regarding claim 3, Ochiai discloses a plurality of third signal lines (CL) formed on the substrate, extending substantially in the first direction, and overlapping the pixel electrodes to form storage capacitors, [fig. 1].

Regarding claim 4, Ochiai discloses wherein the thin film transistors include terminal electrodes connected to the pixel electrodes and overlapping one of the third signal lines with interposing an insulator (ILI), [fig. 3].

Further, Nishimura et al discloses, [fig. 8]:

Claim 2: each of the curved portions of the data lines (DL) comprises a pair of rectilinear portions connected to each other and making an angle of each other about 90 degrees.

Claim 5: the thin film transistors (TFT) include terminal electrodes (SD) connected to the intermediate portions of the second signal lines (DL)

Claim 6: the first signal lines (GL) intersect the intermediate portions of the second signal lines

Claim 37: the angle with respect to the curved portions is about 135 degrees.

Claim 39: the intermediate portions connect curved portions at each end of the intermediate portions.

All of the features in claims 2, 5, 6, 37 and 39 have the same benefit as discussed in claim 1.

Regarding claim 7, Ochiai discloses method of forming a thin film transistor array panel comprising: a substrate (GLS1); a gate line (GL) formed on the substrate and including a gate electrode; a gate insulating layer (GI) formed on the gate line; a semiconductor layer (PSI) formed on the gate insulating layer; a data line (DL) formed on the semiconductor layer at least in part; a drain electrode formed on the semiconductor layer at least in part and separated from the data line; a first passivation layer (PAS) formed on the data line and the drain electrode; and a pixel electrode (SPT) formed on the first passivation layer, connected to the drain electrode, and having an edge extending substantially parallel to the curved portion of the data line, [figs. 1 & 3].

Ochiai lacks disclosure of the data line including a curved portion and an intermediate portion crossing the gate line substantially at a right angle, at least one of the curved portions and the intermediate portions having a source electrode, wherein the intermediate portion extends from the curved portion at an angle with respect to the curved portion.

Nishimura et al discloses the data line (DL) including a curved portion and an intermediate portions crossing the gate line (GL) substantially at a right angle, at least one of the curved portions and the intermediate portions having a source electrode (SD), wherein the intermediate portion extends from the curved portion at an angle with respect to the curved portion, [fig. 8], for the benefit of being possible to obtain multi-domain effect as well as the effect of reducing a parasitic capacity, [par. 0229]. Therefore, at the time the invention was made, it would have been obvious to a person of ordinary skill in the art to have the data line including a curved portion and an intermediate portions crossing the gate line substantially at a right angle, at least one of the curved portions and the intermediate portions having a source electrode, wherein the intermediate portion extends from the curved portion at an angle with respect to the curved portion for the benefit of being possible to obtain multi-domain effect as well as the effect of reducing a parasitic capacity.

Regarding claim 9, Ochiai discloses a storage electrode line (CL) formed on the substrate, extending substantially parallel to the gate lines, and including a storage electrode having an increased width with respect to a width of the storage electrode

line, wherein the drain electrode has an expansion connected to the pixel electrode and overlapping the storage electrode, [fig. 3].

Regarding claim 12, Ochiai discloses wherein the first passivation layer comprises inorganic insulating material, [col. 10, lines 5-6].

Further, Nishimura et al discloses, [fig. 8]:

Claim 8: the curved portion of the data line comprises a pair of portions making a clockwise angle of about 45 degrees and a counterclockwise angle of about 45 degrees, respectively.

Claim 23: a length of the curved portion of the data line is about one to nine times a length of the intermediate portion of the data line

Claim 38: the angle with respect to the curved portion is about 135 degrees.

Claim 40: the intermediate portion connects curved portions at each end of the intermediate portion.

All of the features in claims 8, 23, 38 and have the same benefit as discussed in claim 7.

Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ochiai in view of Nishimura et al, and further in view Kim et al (US 2004/0004280).

Regarding claim 10, Ochiai lacks disclosure of wherein the first passivation layer comprises organic insulating material.

Kim et al discloses the passivation layer comprises organic insulating material having a small dielectric constant for reducing a parasitic capacitance between the pixel electrodes and the data lines, [par. 006]. Therefore, at the time the invention was made,

it would have been obvious to one ordinary skill in the art to have the passivation layer comprises organic insulating material for reducing a parasitic capacitance between the pixel electrodes and the data lines.

Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ochiai in view of Nishimura et al, and further in view of Bae (US 6,337,723).

Regarding claim 11, Ochiai lacks disclosure of wherein the first passivation layer is made of photosensitive material.

Bae discloses the passivation layer is made of photosensitive material for simplifying the manufacturing process because a photo resist is not used and the contact hole can be formed by etching the passivation layer directly, [col. 2, lines 16-19]. Therefore, at the time the invention was made, it would have been obvious to one ordinary skill in the art to have the passivation layer is made of photosensitive material for simplifying the manufacturing process.

Claims 13-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ochiai in view of Nishimura et al, and further in view of Kikkawa et al (US 6,879,359).

Regarding claims 13-16, Ochiai lacks disclosure of a color filter formed on the first passivation layer; wherein the color filter extends substantially parallel to the data line; wherein the color filter has an opening on the drain electrode, the first passivation layer has a contact hole exposing at least a portion of the drain electrode, and the pixel electrode is connected to the drain electrode through the opening and the contact hole; wherein the opening exposes a top surface of the first passivation layer.

Kikkawa et al discloses a color filter (29, 30) formed on the first passivation layer (28) for the benefit of increasing the aperture ratio and performing brighter display, [col. 1, lines 32-37]; wherein the color filter extends substantially parallel to the data line; wherein the color filter has an opening on the drain electrode (26), the first passivation layer has a contact hole exposing at least a portion of the drain electrode, and the pixel electrode (31) is connected to the drain electrode through the opening and the contact hole; wherein the opening exposes a top surface of the first passivation layer, [fig. 1]. Therefore, at the time the invention was made, it would have been obvious to one ordinary skill in the art to have a color filter formed on the first passivation layer (on TFT substrate) for the benefit of increasing the aperture ratio and performing brighter display.

Claims 24 & 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ochiai in view of Nishimura et al, and further in view of Matsuyama et al (US 2001/0006408).

Regarding claims 24 & 25, Ochiai lacks disclosure of a pair of color filters formed on the first passivation layer and partly overlapping each other to form a hill, and further comprising a second passivation layer formed on the color filters and forming a projection on the hill of the color filters.

It was well known to have the color filters partly overlapping each other to form a hill for functioning as black matrix, and forming a projection a projection on the hill of the color filters for functioning as aligning the molecules, as evidenced by Matsuyama et al, [fig. 3A]. Therefore, at the time the invention was made, it would have been obvious to

one ordinary skill in the art to have the color filters partly overlapping each other to form a hill for functioning as black matrix, and forming a projection a projection on the hill of the color filters for functioning as aligning the molecules.

Claims 17 & 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ochiai in view of Nishimura et al, and further in view of Lee et al (US 2001/0026341).

Regarding claim 17, even though Ochiai lacks disclosure of a contact assistant formed on a portion of the gate line or a portion of the data line and made of the same material as the pixel electrode, it was well known to have a contact assistant formed on a portion of the gate line or a portion of the data line for transmitting data or gate signal to the data line or gate line, and the contact assistant made of the same material as the pixel electrode for reducing manufacturing steps as evidenced by Lee et al, [par. 0039]. Therefore, at the time the invention was made, it would have been obvious to one ordinary skill in the art to have a contact assistant formed on a portion of the gate line or a portion of the data line for transmitting data or gate signal to the data line or gate line, and the contact assistant made of the same material as the pixel electrode for reducing manufacturing steps.

Claims 19-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ochiai in view of Nishimura et al, and further in view of Bae (6,337,723) and Matsuyama et al (US 2001/0006408).

Regarding claim 19, Ochiai discloses a second passivation layer (FPAS) made of an organic material, [col. 10, line 7].

Ochiai lacks disclosure of the second passivation layer made of a photosensitive material. However, this limitation is met the discussion regarding claim 11 rejection above in view of Bae.

Regarding claim 20, Ochiai discloses wherein the first and the second passivation layers have a contact hole that exposes at least a portion of the drain electrode and has a sidewall making an angle of about 30 degrees to about 85 degrees with a surface of the substrate, and the pixel electrode is connected to the drain electrode through the contact hole, [fig. 3].

Regarding claim 21, even though Ochiai lacks disclosure of a contact hole that exposes at least a portion of the drain electrode having a stepped sidewall, it would have been obvious to one ordinary skill in the art to change the shape of the element, [MPEP 214404.IV.B Changes in Shape]. Further, having stepped sidewall contact hole would still have the main function as contacting and therefore does not patentably distinguish over the invention.

Regarding claim 22, Ochiai discloses wherein entire bottom surfaces of the data line and the drain electrode are disposed substantially on the semiconductor layer, the data line and the drain electrode have substantially the same planar shape as the semiconductor layer, and the semiconductor layer includes a portion that is not covered with the data line and the drain electrode and disposed between the source electrode and the drain electrode, [to form a channel in TFT, fig. 3].

Response to Arguments

Applicant's arguments with respect to claims 1-25 and 37-40 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL.** See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Contact Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to (Nancy) Thanh-Nhan P. Nguyen whose telephone number is 571-272-1673. The examiner can normally be reached on Monday to Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Nelms can be reached on 571-272-1787. The fax phone number for

the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

(Nancy) Thanh-Nhan P Nguyen
Examiner
Art Unit 2871

TN

David Nelms
Supervisory Patent Examiner
Technology Center 2800